REMARKS

Applicants appreciate the Examiner's thorough review of the present application, and respectfully request reconsideration in light of the preceding amendments and the following remarks.

Several claims have been amended to better define the claimed invention. New claim 31 has been added to provide Applicants with the scope of protection to which they are believed entitled. No new matter has been introduced through the foregoing amendments.

The claim objections are believed overcome in view of the above amendments which have been made in the manner kindly suggested by the Examiner in the Office Action.

The *35 U.S.C. 112, second paragraph* rejection is also believed overcome in view of the above amendments. In particular, claims 28-29 are now dependent on claim 26 which recites the "input terminal" in the first line.

The repeated *35 U.S.C. 103(a)* rejection of all claims are noted, and traversed for at least the reasons presented in the previous Amendment(s) which are incorporated by reference herein for the sake of simplicity.

In addition, Applicants respectfully submit that the primary reference of *Naganuma* and the teaching reference of *Bui* are not properly combinable. *Naganuma*, as correctly noted by the Examiner, discloses time constant circuits 61, 62. *Bui*, on the other hand, discloses a time delay circuit in FIG. 8A. A person of ordinary skill in the art would understand that the time constant circuit of *Naganuma* and the time delay circuit of *Bui* are designed for two different purposes and would not be combinable and/or interchangeable. In particular, the time constant circuit of *Naganuma* is provide to control the speed at which the gate voltages of the FETs 71, 72 change. *See Naganuma* at column 4 lines 42-45, 65-68, column 5 lines 40-54. The time delay circuit of *Bui* is provided to shift the output signal in time relative to the input signal. To place the *Bui* time delay

circuit in the time constant circuit of *Naganuma* as proposed by the Examiner would add no advantage to *Naganuma* as the output of FETs 71, 72 will be merely delayed, resulting in an unnecessary retardness in the response time of the circuit and adversely affecting the processing speed of the *Naganuma* device. Thus, the person of ordinary skill in the art would not have been motivated to combine *Naganuma* with *Bui* as suggested by the Examiner.

Notwithstanding the above and solely for the purpose of expediting prosecution, Applicants have further amended the claims to specifically avoid the Examiner's improperly combined references.

In particular, **independent claim 1** now recites, among other things, that "said one of the first and second transistors is switched from off to on before said at least one voltage responsive switchable capacitor is switched from the initial finite capacitance value to the substantially open circuit." The claim now defines a relationship between the switchable capacitor and the corresponding transistor.

The new claim feature finds support in at least FIG. 2 and the corresponding text in the specification, e.g., paragraphs 0031-0032 of the published application where it is disclosed that NFET 50 is switched from off to on at about 0.33 Vdd (near 72 in FIG. 2), i.e., before capacitor 34 is switched from the initial finite capacitance value to the substantially open circuit at about 0.67 Vdd (near 78 in FIG. 2). A similar teaching can be found in paragraph 0034 of the published application where it is disclosed that NFET 48 is switched from off to on at about 0.67 Vdd (near 86 in FIG. 2), i.e., before capacitor 32 is switched from the initial finite capacitance value to the substantially open circuit at about 0.33 Vdd (near 88 in FIG. 2). An advantage of embodiments implementing the claimed invention has been disclosed in paragraph 0032 of the published application.

In the combined device of *Naganuma* and *Bui*, there is no disclosure or suggestion of any relationship between the switchable capacitor 807/808 (*Bui*) and the corresponding transistor 71/72 (*Naganuma*). Due to the non-enabling disclosure of *Bui*, a person of ordinary skill in the art would

have found no suggestion or motivation in the art to further modify the combined device to include the newly claimed relationship. Accordingly, Applicants respectfully submit that amended independent claim 1 is patentable over the applied art of record.

Independent claims 22 and 26 have been amended to include a limitation similar to the above-discussed feature of amended claim 1. Independent claims 22 and 26 are, therefore, also believed patentable over the applied art of record.

The **dependent claims**, including new claim 31, are considered patentable at least for the reasons advanced with respect to the respective independent claims.

Each of the Examiner's rejections has been traversed. Accordingly, Applicants respectfully submit that all claims are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the present application should be in condition for allowance and a Notice to that effect is earnestly solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 08-2025 and please credit any excess fees to such deposit account.

Respectfully submitted,

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